ABSTRACT OF THE DISCLOSURE

A pulse duty deterioration detection circuit with a high monitoring precision is easily provided. The pulse duty deterioration detection circuit comprises a delay circuit comprised of a general-purpose gate circuit which generates a delayed synchronous to-be-monitored clock by delaying the to-be-monitored clock by a predetermined time, a latch circuit which detects based on the to-be-monitored clock and the delayed synchronous to-be-monitored clock that a value of a decrease in a pulse width to be determined by a pulse duty of the to-be-monitored clock becomes smaller than the predetermined time, and a flip-flop circuit which samples an output signal of the latch circuit based on the to-be-monitored clock.